In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the new mandatory amendment format.

1. (Previously Presented) A method comprising:

receiving real-time analog data at a personal computer implementing a general purpose operating system;

generating a real-time interrupt indicating a request to process the real time data at a central processing unit (CPU);

determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at the CPU; and

processing the real-time data if the real-time interrupt has a higher priority than the non-real time operation.

2. (Previously Presented) The method of claim 1 further comprising continuing to process the non-real time operation if the real-time interrupt does not have a higher priority than the non- real time operation.

3. (Previously Presented) The method of claim 1 further comprising:

saving the state of the non-real time operation at the personal computer prior to processing the data associated with the real-time interrupt; and

processing the non-real time operation after processing of the data associated with the real-time interrupt has been completed.

4. (Previously Presented) The method of claim 1 further comprising:

receiving a non-real time interrupt while processing the real-time interrupt; and

determining whether the non-real time interrupt has a higher priority than the real-time interrupt.

5. (Previously Presented) The method of claim 4 further comprising:

continuing the processing of the real-time interrupt if the non-real time interrupt does not have a higher priority than the real time interrupt.

6. (Previously Presented) The method of claim 4 further comprising:

terminating the processing of the real-time interrupt if the non-real time interrupt has a higher priority; and

processing the non-real time interrupt.

7. (Previously Presented) A computer system comprising:

a chipset;

a bus coupled to the chipset; and

a central processing unit (CPU), coupled to the bus, to generate a real-time interrupt upon receiving real-time analog data and to process data associated with the real-time interrupt if the real-time interrupt has a higher priority than a non-real-time operation currently being processed.

8. (Previously Presented) The computer system of claim 7 wherein the CPU comprises:

a timer to generate timing signals at predetermined time intervals; and

an event mechanism coupled to the timer to generate the real time interrupts.

9. (Previously Presented) The computer system of claim 8 wherein the CPU further comprises an event handler coupled to the event mechanism to process the real-time interrupts.

10. (Original) The computer system of claim 9 wherein the CPU further comprises a register coupled to the event mechanism to store real-time data.

11. (Previously Presented) The computer system of claim 9 wherein the event mechanism determines the relative priority between the real-time interrupts and the non-real-time operations.

12. (Original) The computer system of claim 11 wherein the CPU further comprises an analog to digital converter coupled to the register.

13. (Previously Presented) A central processing unit (CPU) comprising:

a timer to generate timing signals at predetermined time intervals;

a register to store real-time data received at the CPU as analog data;

an event mechanism coupled to the timer and the register to generate real time interrupts in response to receiving the timing signals and determining that real-time data is stored within the register; and

an event handler coupled to the event mechanism to process data associated with the real-time interrupts received from the event mechanism upon determining the relative priority between the real-time interrupts and non-real-time operations being processed.

14. (Previously Presented) The CPU of claim 13 wherein the real-time analog data is data received from an analog radio coupled to the CPU.

15. (Previously Presented) The CPU of claim 13 wherein the event handler verifies whether there is data stored in register upon detecting a real-time interrupt and determines the priority of the real-time interrupt relative to other interrupts received.

16. (Previously Presented) The CPU of claim 13 wherein the CPU further comprises an analog to digital converter coupled to the register to convert the real-time analog data to digital data.

17. (Previously Presented) The method of claim 1 wherein receiving the real-time analog data comprises:

converting the real-time analog data to digital data; and

storing the digital data at a register.

18. (Previously Presented) The method of claim 17 wherein generating the real-time interrupt comprises:

receiving a timing signal at an event mechanism at a predetermined interval;

the event mechanism determining whether data is stored within the register; and

generating the real-time interrupt if data is stored within the register

19. (Previously Presented) The computer system of claim 10 wherein the event mechanism generates the real time interrupts in response to receiving the timing signals from the timer and determining that real-time data is stored within the register.

20. (Previously Presented) The computer system of claim 7 wherein the real-time analog data is data received from an analog radio.